38. (New) The semiconductor die as recited in claim 35, wherein the planar edges have ground surfaces.

39. (New) The semiconductor die as recited in claim 35, wherein the planar edges have polished surfaces.

40. (New) The semiconductor die as recited in claim 35, wherein the planar edges are substantially parallel to one another.

41. (New) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar edges, where the planar edges are substantially transverse to the first planar surface or the second planar surface; and

each planar edge has a flat, smooth surface.

42. (New) The semiconductor die as recited in claim 41, wherein the semiconductor die comprises a rectangular die.

43. (New) The semiconductor die as recited in claim 41, wherein the planar edges are substantially parallel to one another.

Claims 11-25 and 35-43 are now pending in this application. The Examiner is invited to contact the below-signed attorney with any questions regarding the present application.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 29 day of June, 2001.

Tina Pugh
Name

_____
Signature